High Performance On-Chip Array Antenna Based on Metasurface Feeding Structure for Terahertz Integrated Circuits

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***Abstract*: In this letter, a novel on-chip array antenna with high-performances is investigated which is based on CMOS 20µm Silicon technology for operation over 0.6-0.65 THz. The proposed array structure is constructed on three layers composed of Silicon-Ground-Silicon layers. The ground-plane has sandwiched between two silicon layers. Two antennas are implemented on the top layer, where each antenna is constituted from three sub-antennas. The sub-antennas are constructed from interconnected dual-rings. Also, the sub-antennas are interconnected to each other. This approach enlarges the effective aperture area of the array, which has caused to improve its performance parameters. Surface waves and substrate losses in the structure are suppressed with the metallic via-holes that have inserted through the three layers and implemented between the radiation elements. To excite the structure, a novel feeding mechanism is used comprising open-circuited microstrip lines located on the back side of the structure, which couple the electromagnetic energy from the bottom layer to the antennas on the top-layer through metasurface slot-lines in the middle ground-plane layer. The results show the proposed on-chip antenna array has an average radiation gain, efficiency, and isolation of 7.62 dBi, 32.67%, and -30 dB, respectively.**

I. INTRODUCTION

Recently, the electromagnetic spectrum in the terahertz (THz) band has attracted great interest because of its potential applications in imaging, radio astronomy, spectroscopy, security control and communications. In such systems an antenna plays an important component to interface the terahertz signal with free-space. Various THz antennas have been reported in the literature including dipole antenna, spiral antenna, graphene antenna, leaky wave antenna, on-chip antenna, Yagi-Uda antenna and butterfly shaped antenna [1-7]. Close examination of these antennas reveals their limitations, particularly in the way they interact with electromagnetic waves for optimum impedance matching necessary for effective detection and their construction [8-13].

In this letter, proposed is an array antenna that is based on CMOS 20µm Silicon with properties of small dimensions, low profile, design simplicity and ease of implementation. The results presented demonstrate that the antenna exhibits a wide impedance bandwidth with relatively high radiation gain and efficiency. In addition, the isolation between the array's radiation elements is high, which makes it suitable for integrated circuits for terahertz applications. The proposed structure employs a novel feeding mechanism that is based on metasurface slot-lines.

II. ON-CHIP ARRAY ANTENNA DESIGN WITH A NOVEL FEEDING MECHANISM

Fig.1 shows the proposed on-chip array antenna constructed of two 20µm Silicon layers that sandwich a 20µm ground plane (GND). Two microstrip antenna structures are implemented on the top Silicon layer. Each antenna structure is composed of three sub-antennas, which are made of interconnected dual rings of different diameters. The three sub-antennas are connected to each other to enhance the arrays radiation properties. With this approach the effective aperture of the antenna is enlarged thereby enhancing its radiation characteristics. Surface waves and substrate losses in the structure are suppressed with metallic via-holes that have inserted through the three layers and implemented between the radiation elements. The antennas are exciting using a novel feed mechanism based on electromagnetically coupling energy from bottom layer to top layer. The bottom side of the on-chip array antenna with two open-ended microstrip lines is shown in Fig.1. In the GND plane the slot-lines are etched to facilitate electromagnetic coupling of energy from the bottom to the top layer. The slot-lines in the GND plane are designed based on metasurface technique.

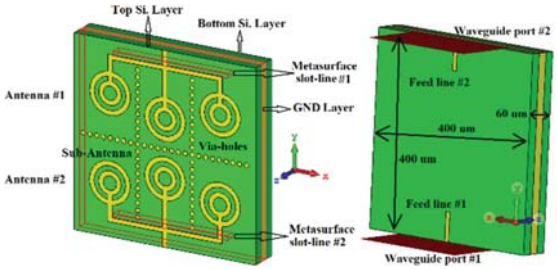

Fig.1. Proposed on-chip array antenna prototype in different views.

S-parameter responses of the proposed array antenna is shown in Fig. 2. The response covers the frequency range from 0.6 THz to 0.65 THz, which is corresponded to a fractional bandwidth of 8%. In addition, the isolation between the array elements is better than 20 dB over this frequency range, which illustrates the effectiveness of this array at detecting THz

signals.

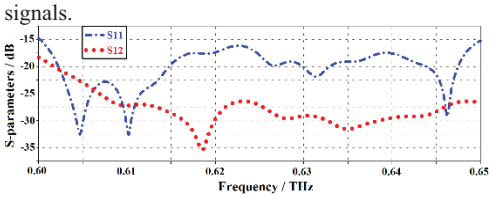

Fig.2. Reflection (S_{11}<-15dB) and transmission coefficients (S_{12}<-20dB) of the proposed on-chip array antenna.

The radiation gain and efficiency performances over the frequency range of 0.6 THz to 0.65 THz is shown in Fig.3. The maximum gain and efficiency observed at 0.63 THz are 8.1 dBi and 38.24%, respectively.

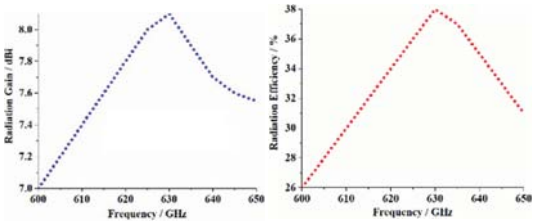

Fig.3. Radiation gain and efficiency plots.

To increase the validity of the proposed design, it has compared with the recent papers. The results are summarized in Table I. It is clear that, the proposed on-chip antenna shows better performance parameters than the referenced papers.

TABLE I. COMPARISON TABLE

Ref.	Antenna Type	Freq. (GHz)/ BW (%)	Gain (dBi)	Eff. %	Process	Size (mm^2)	Height (mm)
[1]	Patch Fed Higher Order Mode DRA	341/7	7.9	74	0.18-μm SiGe	0.2	0.5
[2]	On-chip 3D (Yagi like concept)	340/12	10	80	0.13-μm SiGe	0.49	0.11
[4]	Slot-Loaded Magnetic Loop on SIW	340/7	3.3	45	0.13-μm SMOS	0.49	-
[7]	Patch	280/2.5	–1.6	21	0.13-μm CMOS	0.2	-
[8]	Ring Antenna	296/-	4.2	-	65-nm CMOS	0.3	-
[9]	Slot Ring Antenna + Superstrate	375/8	1.6	35	45-nm CMOS SOI	0.05	-
[10]	Ring Antenna with Silicon Lens	288/NA	18.3	65	65-nm CMOS	12.56	2.55
[11]-a	Half-Mode Cavity Fed DRA	135/13	3.7	62	0.18-μm CMOS	0.63	0.25
[11]-b	Half-Mode Cavity Fed Higher Order Mode DRA	135/7	6.2/7.5	46/42	0.18-μm CMOS	0.72	1.3/2.2
[12]	Slot Fed Stacked DRA (Two DRAs + Supporter)	130/11	4.7	43	0.18-μm CMOS	0.72	1.28
[13]	DRA	135/11	2.7	43	0.18-μm CMOS	0.72	0.6
This Work	Metasurface	630/8	8.1	38.24	CMOS	0.16	0.06

III. CONCLUSION

Feasibility of an on-chip array antenna that exhibits high radiation gain and efficiency characteristics is demonstrated across a wide terahertz bandwidth between 0.60 THz to 0.65 THz. The array antenna is implemented on CMOS 20µm Silicon layers. Isolation between the sub-antennas constituting the array was increased by implementing metallic via-holes between the radiation elements. The array was excited electromagnetically from the bottom layer using a novel feeding mechanism based on metasurface slot-lines realized inside the middle ground plane layer. The results reveal the viability of the array antenna for THz integrated circuits.

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