Investigations in the Modelling and Control of a Medium Voltage Hybrid Inverter System that uses a Low Voltage /Low Power rated Auxiliary Current Source Inverter

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***Abstract*— Hybrid converters consist of a main inverter processing the bulk of the power with poor waveform performance and a fast and versatile auxiliary inverter to correct the distortion. In this paper, the main converter is a medium voltage NPC inverter and the auxiliary inverter is a low-voltage and low-current rated current source inverter (CSI), with series capacitor being used to minimize the CSI voltage stress. The result is a high output current quality which is obtained with a very low switching stress in the main converter and a very small added installed power (<4%) in the CSI. This paper expands this concept by investigating the hybridization of a medium voltage inverter with an existing LCL filter and investigates the additional challenges related to resonances and proposes a solution for stable operation. Experimental validation of active ripple cancellation has been provided at 3kW.**

***Index Terms*— Active filters, Noise cancellation, Nonlinear filters**

I. Introduction

Conversion of DC into AC at medium and high voltage levels has become a very important research topic now when the need to transfer very large amounts of power (GW) over long distances favour HVDC transmission systems. In the medium term it is predicted that the distribution system will remain AC which will require the use of high voltage DC/AC inverters to interface the transmission and distribution systems. Standard two-level inverters built using series connected devices were initially used in the first generation of forced commutated HVDC systems for their simplicity and the easiness to embed redundancy by adding additional devices in series; however, difficulties in achieving static and more importantly dynamic voltage sharing during switching meant that the harmonic performance of such inverters was poor due to reduced voltage levels and further limited by the low switching frequency. In the last 5 years, forced commutated IGBTs with ratings of 6.5kV[1] became commercially available which would reduce the number of series connected devices needed in a two-level inverter and therefore lower complexity and cost. However, the poorer switching performance of a medium voltage (voltage rating >2kV) forced commutated device which for same kVA switched, results in higher switching loss, is also a limiting factor that will limit the switching frequency to approximately 1 kHz, which means power quality will remain a problem for a two-level medium/high voltage inverter implementation.

Multilevel voltage inverter topologies [2-5] such as the cascaded H-bridge, the flying capacitor and the diode clamped inverters proposed more than 15 years ago, promised to solve the limitations of the inverters using series connected switches but their application was limited in practice to a low number of levels (three as is the case of the NPC inverter). The most important drawbacks were that the modulation and control became very complex and also that building of an inverter leg with high number of levels requiring different connection paths for the clamping diodes or capacitors that resulted in large and uneven stray inductances made the implementation of building blocks quite difficult. The Modular Multilevel Converter (MMC) proposed few years ago [6, 7] has gained increased popularity in a short period of time due to its reliance on a large number of identical building blocks that would enable cost effective mass production and allow flexibility in implementing any custom design system solutions. Hybrid converter implementations have been proposed in the past to enhance the behaviour of passive filters [8, 9] or to improve the waveform quality of slow converters by adding low current rated auxiliary converters [10-17].

In [13] the authors of this paper have proposed a hybrid solution aimed at improving the harmonic performance of a slow switching medium/high voltage inverter by means of employing an auxiliary current source inverter with very low installed power to cancel the switching harmonics caused by the main converter. The CSI is used because it is very good at synthesizing an AC current reference, in this case the switching current ripple which is in the hundreds Hz range of the main MV inverter, with the lowest switching frequency. A series capacitor to block most of the fundamental (50Hz) voltage is connected in series with the CSI to minimize its voltage ratings so standard/fast switches (ratings up to 1.2kV) could be used.

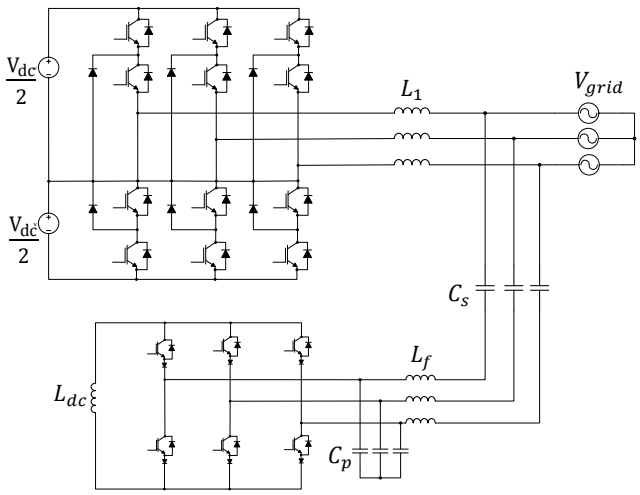

Figure 1: Hybrid converter topology connected to a stiff grid

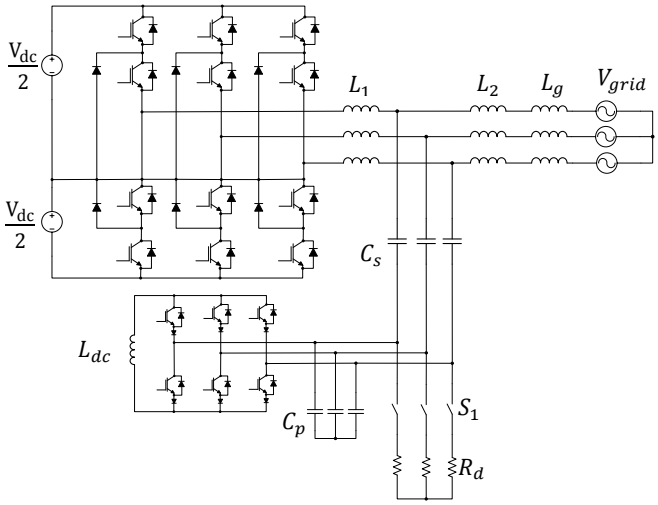

Figure 2: Hybrid converter topology with LCL filter interconnection

The proposed hybrid concept shown in Fig. 1 is similar to [10] where the auxiliary inverter cancels the main current switching ripple which is a fraction of the main inverter current. With respect to the hybrid filter idea, most papers are using a Voltage Source Inverter as the auxiliary bridge which if used to synthesize currents would require a fast current controller and for that reason very fast switching. A VSI with a hysteresis controller could be used as an alternative solution however the wide harmonic spread of a hysteresis controller makes it more likely to excite oscillation of LC circuits which form the switching harmonic filters making them less appropriate for grid connected applications. Although the weight of DC-link inductor of the CSI tends to be larger compared to DC-link capacitor of VSI, the inductor lifetime and its ability to handle surge stresses (overcurrents/overvoltages) is superior compared to electrolytic capacitors which are more sensitive to overvoltages, current ripple and temperature variations.

[11] has demonstrated the idea of implementing a medium voltage active filter by using a low voltage 3-phase voltage source active power filter (APF) in series with a capacitor to minimize/block the 50Hz fundamental component voltage stress across the converter whilst also minimizing the cost. The use of a series capacitor with a CSI has been investigated in [12, 18] but for low voltage APF applications and in [19]for photovoltaic applications. The novelty in relation to [10] is that it addresses medium/high voltage applications and that the installed power of the auxiliary inverter is further reduced by using a series connected capacitor to cancel most of the fundamental (50Hz) AC voltage, similar to [11]. By using a current source inverter (CSI) as in [12] the circuit does not need the current controllers that a VSI would need in an active filter application, since the AC reference currents are synthetized directly, therefore, being able to switch slower for a similar current tracking performance.

The second section of this paper briefly outlines the design procedure followed in [13] for the Hybrid converter in a medium voltage stiff grid application, revealing the key results and system scaling considered necessary for the reader to familiarize with the context and operation of the Hybrid concept. The third section outlines the procedure followed into designing the LCL filter and CSI along with the design considerations taken and alterations compared to the previous design. The fourth section outlines the options for damping resonant frequencies and proposes an active damping compensator before showing the simulation results that validate the expected operation of the hybrid system. An increase in complexity of the system to account for the mitigation of the voltage ripple seen at the input terminals of the hybrid system (equivalent to point of common coupling – PCC) caused by the CSI switching harmonics, along with an evaluation of the sensitivity to wide grid impedance variation is also included. The impact on efficiency is explored by estimating the semiconductor losses. The final section shows experimental behaviour of the system, currently in development, at 3kW with the performance analysed to validate simulated results.

II. LCL CONNECTED HYBRID TOPOLOGY

This paper expands on previous work relating to the Hybrid concept in [13] by investigating the challenges of applying the same technique to connect the auxiliary CSI via series capacitors to the MV grid/main inverter via their split inductance that typically will form an LCL filter and lead to the known associated stability problems reported already in literature[20]. The resulting topology is shown in Fig. 2. It contains also a set of damping resistors and a contactor that can be used to switch the main VSI operation mode from passive LCL filtering of the switching current ripple to active/hybrid operation.

The evolution from the Hybrid topology shown in Fig. 1, which assumes an ideal stiff grid, to the LCL connected Hybrid topology in Fig. 2 comes as a logical progression when taking into account the supply line inductance. This could be considered a more realistic implementation for medium voltage (and perhaps weaker) grids, as the grid line inductance will naturally form an output LCL filter when combined with the series capacitance and VSI side inductance. The other

advantage is that the inductor L_f present in the CSI filter shown in Fig. 1 is no longer necessary.

LCL filters are known to achieve better attenuation compared to a 1st order (L) filter with smaller component size however their design is more challenging due to the need to carefully consider the resonant frequency placement and the potential damping of resonances. LCL filter design for medium voltage applications is even more restricted by the low converter switching (around 1kHz) frequency [21, 22] therefore requiring the filter resonant frequency to be placed close to the typical low order harmonics(5th, 7th etc) present in distribution grids. The problem is outlined in [21] where the concept of virtual harmonic content is introduced in order to design the LCL filter to comply with grid code requirements with the lowest possible filter size whilst [10] proposed the additional use of the computationally demanding selective harmonic elimination PWM (SHE-PWM) to eliminate harmonics up to the 29th order to allow for higher resonant frequency placement and therefore achieve smaller filter size. Although in this paper, a more simplistic approach was taken towards the LCL filter design, the considerations are in line with existing literature [20-22].

The connection of the CSI operating as an Active Power Filter (APF) on an existing LCL filter can achieve further improvement in the harmonic current filtering with very low added installed power with the potential of adding only the auxiliary CSI, its AC side filter capacitor C_p and the overvoltage protection, with no other additional components (AC side inductors). The resulting topology shown in Fig. 2 allows for two modes of operation via switch S1. When the switch is closed and the CSI disabled, the VSI operates using passive LCL filtering with the resistors R_d providing damping. When the switch is opened and the CSI is enabled, the circuit operates as a Hybrid active filter with the damping resistor R_d and its associated losses removed. As a result the overall topology can be considered hybrid in two ways, due to the combination of a main VSI and auxiliary CSI as well as the option of choosing between passive and active filtering.

Switch S1 in this simulation study is used to compare the harmonic performance between passive and active filtering. Realistically it could be implemented as a mechanical or electronic (Triac) switch depending on the functionality needed: redundancy or safe start-up/shut-down(inrush current limitation). Although the switch could be realized with semiconductors there is no clear advantage given that it must be rated at the full grid voltage and more than 20% of the current. An electromechanical switch (contactor) would be sufficient to provide the required protection, synchronization and meet the ratings at a reduced cost.

The addition of the CSI to the LCL has two main topological implications. During active filtering, the damping resistor R_d of the LCL filter is no longer needed therefore a source of resistive losses is removed. Compared to the stiff grid design, the AC side filter inductor of the CSI (L_f) are no longer necessary as sufficient attenuation is achieved by the combination of capacitor C_p and grid side inductance. The unexpected benefit of this is that, when using a stiff grid connection this filter favoured high CSI switching frequencies to maintain small component size. However, as the large enough grid side inductance is present in an LCL filter, a lower switching frequency of the CSI can give the same performance.

III. Design of the Hybrid System Connected to a Stiff/Ideal Grid

The circuit topology, shown in Fig. 1, consists of a slow switching medium voltage three level Neutral Point Clamped (NPC) VSI as the main bridge that interconnects with the MV grid via a line side inductance L_1 that is designed to limit the switching current ripple while the Series Capacitor Active Power Filter APF auxiliary bridge is a three phase two level CSI connected in series with a capacitor (C_s) that is designed to block most of the 50Hz voltage. Capacitor C_p along with L_f and R_f (not shown) is the CSI second order low-pass AC side filter necessary to smooth the PWM output current of the APF. The control of the main VSI is independent to the CSI and can remain largely unchanged compared to a standalone VSI installation. The CSI primary role is to act as an active filter to the switching current ripple produced by the VSI. By also injecting a calculated fundamental current in the series capacitor it is possible to control the fundamental voltage drop on the capacitor and therefore ensure minimal voltage stress on the CSI. The reference waveform to the CSI is therefore the switching current ripple of the main bridge which can be sensed and the calculated reactive fundamental current component to achieve the desired voltage drop. The detailed hybrid converter model including the phasor diagrams used to derive the control and the design equations are detailed in [13]. In Table I, the specifications for the hybrid converter used in this simulation study are summarised.

TABLE I: SPECIFICATIONS FOR MEDIUM VOLTAGE HYBRID SYSTEM DESIGN

$V_{g\,L-L}$	I_g	$V_{g\,ph}$	Vdc	S	ΔI_{max}	f_{sw}^{VSI}	f_{sw}^{CSI}
3.3 kVrms	330 Arms	2.7 kVpk	2x3 kV	1.89 MVA	94 A	1 kHz	30 kHz

A. Design Procedure Outline

The converter side inductance L_1 has been designed by limiting the maximum current ripple in the inverter side inductance L_1 to 20% of the peak to peak maximum current. This maximum current ripple is calculated based on the VSI DC link voltage level and the modulating strategy chosen for a given topology.

Fig. 3 reveals the simplified phase equivalent circuit at the fundamental and VSI switching frequency. The series capacitor C_s design is designed based on various requirements. A smaller series capacitance results in lower reactive current requirement to achieve a given fundamental voltage drop however this is counteracted by the larger switching voltage drop (1) across the series capacitor which is mirrored equally at the AC side of the CSI as shown in Fig. 3b.

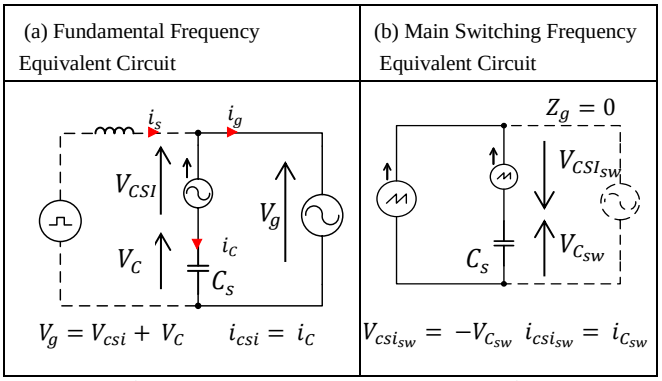

Fig. 3. Simplified phase equivalent circuit at a) the fundamental grid frequency and b) VSI switching frequency

To ensure that the series capacitance meets the design requirements, the minimum value is calculated based on (2) for a maximum switching voltage stress while the maximum value is based on limiting the maximum reactive power requirement on the VSI (3) to minimise the effect on the output power factor.

$$V_{csi_{sw}}^{ln} = |i_{sw}|X_c = \frac{|i_{sw}|}{\omega_{sw} C_s} = -V_{c_{sw}}^{ln} \quad (1)$$

$$C_{s_{min}} = \frac{|i_{sw}|}{\omega_{sw}|V_{c_{sw}}|} \quad (2)$$

$$C_{s_{max}} = \left(\frac{Q}{S}\right)\frac{\sqrt{3} i_s^{RMS}}{V_g^{RMS}\omega} \quad (3) \qquad G = 1 + \frac{C_p}{C_s} \quad (4)$$

The parallel capacitance C_p is chosen to be large enough to smooth the CSI PWM current however must be kept as small as possible to reduce the amount of circulating current which is based on the ratio of series and parallel capacitances (4). The switching current reference to the CSI must be multiplied by a gain (4) to compensate for that bleeding current. The inductance L_f and resistance R_f are subsequently chosen to form a second order low pass filter with cut off frequency at half the CSI switching frequency or less in order to achieve sufficient attenuation. In this case the filter has been designed for a cut-off frequency of 10 kHz.

The maximum voltage stress on the CSI has been chosen as 20% of the peak grid voltage (940$V_{L\text{-}L\text{-}pk}$), with half being caused by the fundamental voltage (V_g-V_{Cs}) and the other half (10%) caused by the switching current ripple across C_s which is mirrored also across the CSI AC input. This design scenario results in the minimum value for C_s. Limiting the reactive power as percentage (20%) of the apparent power defines the other limit for the series capacitor range, which in this case is 55-110µF. In Table II shows all the parameters for the design procedure with stiff grid.

TABLE II: DESIGN PARAMETERS FOR HYBRID CONVERTER WITH STIFF/IDEAL GRID

$C_{s\ min}$	$C_{s\ max}$	L_f	R_f	L_{dc}
55µF	110µF	23µH	10Ω	20mH
C_p	L_1	V_{sw} max @55 µF	V_{csi} max	I_{dc} @ C_s @55/110 µF
11µF	3.6mH	470V	940Vpk	140/184

B. Control Scheme of the Hybrid Converter

The control of the CSI is implemented according to the diagram shown in Fig 5. The switching current ripple is extracted from VSI inductor L_1 current per phase, removing any low order harmonics or DC components and multiplied by (4) to compensate for the fraction of the CSI current that is trapped by the CSI filter capacitors C_p. The fundamental current component is calculated in the *dq* rotating frame with the active component contributing towards maintaining the DC-link current above the peak of the AC current reference and the reactive component to achieve the desired capacitor voltage drop and synchronised with the grid voltage. Finally a DC voltage compensator is added to protect the CSI and series capacitor voltages from the possibility of DC drifting.

C. Simulation results of Hybrid Converter with stiff grid

The simulation results of the hybrid converter operating with stiff grid are presented in Fig 4 for a series capacitance of 110µF. The CSI maximum voltage stress is below 20% of the line to line grid voltage with the Capacitor and CSI phase voltages shown together in Fig. 5b, for comparison. The grid current THD has been calculated at 2% compared to 11% THD of the VSI side current, achieving a 96% reduction in the main switching frequency harmonic and all current harmonics being kept below 1% of the fundamental current. The installed power in the CSI is maintained below 4%.

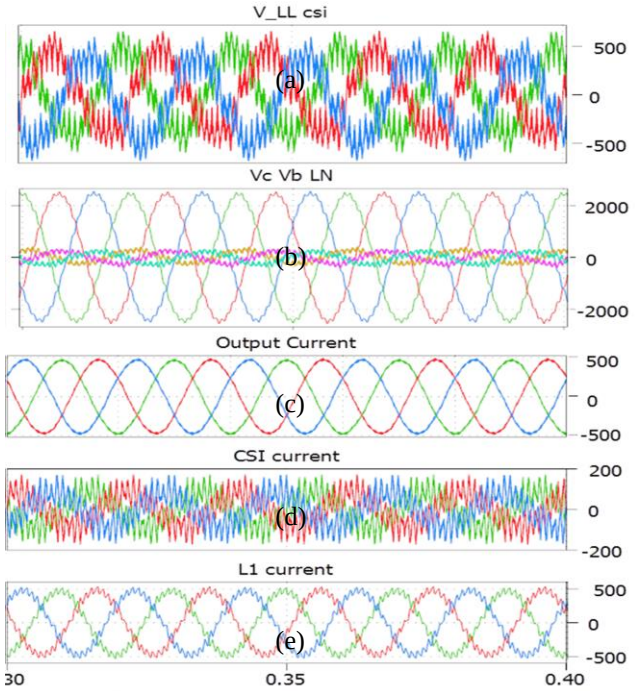

Fig. 4. Hybrid converter connected to a stiff grid: a) AC L-L voltages of the CSI; b) Series capacitor (large) and CSI phase voltages; c) resulting grid currents; d) injected currents by the CSI; e) main VSI currents.

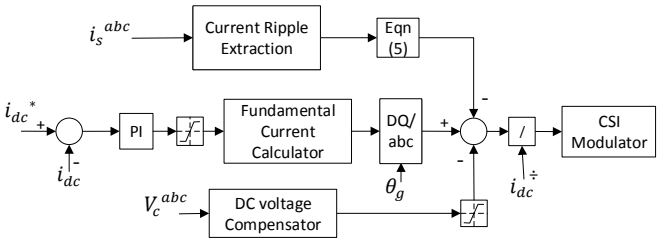

Fig. 5. Control scheme overview

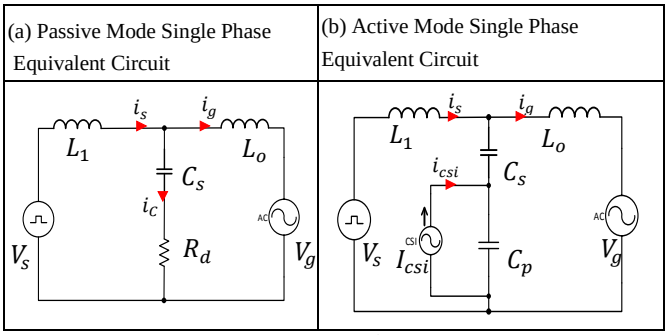

Fig. 6. Single Phase equivalent circuits for a) Passive; b) Active Filtering

IV. Hybrid System Connected via LCL Filter

The following section outlines the additional design considerations along with the procedure required to obtain a stable performance when the hybrid converter is connected to the grid via an LCL filter under the same requirements for the maximum CSI voltage stress and grid specifications. Since the system in Fig 2 can operate as two different circuits, they will be treated as such in the design procedure and referred to as Passive mode, when the switch S1 is closed and CSI is disabled and Active mode when S1 is open and CSI is enabled. The procedure starts by designing the LCL circuit, ensuring proper Passive mode operation. The focus of the paper is afterwards centred on the design of the CSI and the choices made in order to meet the aforementioned design requirements. The single phase equivalent circuits for each mode are shown in Fig. 6 where the inductances of the LCL output and grid side (L_2 and L_g) are grouped as a single inductance L_o to reflect the frequency response of the system.

A. LCL Filter Design Procedure

The VSI inductance L_1 is chosen to limit the maximum switching current ripple at 20% giving the same value as in the stiff grid situation of 3.6mH. The Grid side impedance is then calculated based on [23] for a *SCR*= 10 and *X/R* = 5 resulting in L_g=1.8mH and R_g=0.113Ω. This values have been chosen to be representative of a near weak grid situation, usually identified as having a SCR lower than 10, to reflect the possibility of the system operating in non-ideal grid situations. The inductance L_2 is chosen at 1.8mH so that L_g+L_2 match the converter side inductance therefore avoiding extra resonances in the system.

The LCL/series capacitor C_s must then be chosen to place the resonant frequency (5) at approximately half of the switching frequency or below. The maximum capacitance value is usually restricted based on the allowed reactive power generated therefore a similar range of capacitances for C_s can be considered as the previous design i.e. 55-110μF with respective resonant frequencies between 500-360Hz

$$\omega_{res1}=\frac{1}{\sqrt{L_t C_s}} \quad \text{where } L_t=\frac{L_1 L_o}{L_1+L_o} \quad (5)$$

For the following design, a value of 100μF has been chosen to enable lowest consumption of CSI installed power devices, as detailed in [13] where it was shown that the result of the Cs versus CSI installed power optimisation is convergent even when a large range of CSI losses are considered as seen in Fig. 7a and 7b under the assumption that the CSI efficiency typically ranges from 85%-95% of the apparent power processed, depending on switching frequency. The results are shown for a range of series capacitor values with each curve representing different DC-link resistance equivalent to 5, 10 and 15% loss of the apparent power processed. By using 100μF the resonant frequency of the resulting LCL filter is 375Hz. A damping resistor R_d=50mΩ has been chosen to give sufficient damping and very good attenuation of the 1 kHz switching frequency ripple.

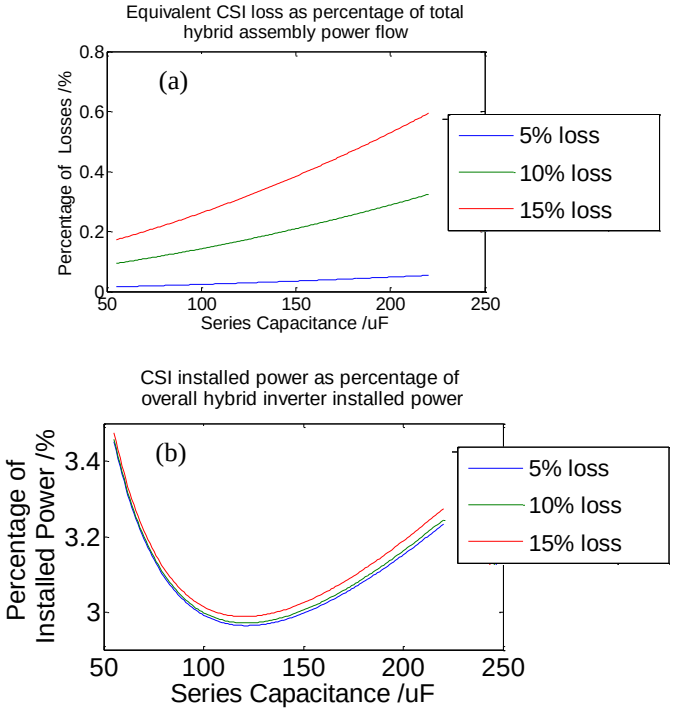

Fig. 7: a) CSI Losses as percentage of hybrid system loss and b) Added Installed Power versus size of Series Capacitance at different DC-link resistance equivalent to 5-10-15% loss of processed apparent CSI power.

B. CSI Active filter design

The connection of the CSI and its filter capacitor C_p in neutral point of the LCL filter presents a convenient place from the point of view of maintaining low voltage insulation and voltage CSI ratings, as the neutral potential is closest to ground but leads to an intriguing design problem to provide stable operation. In addition to the CSI design restrictions

existent for the stiff grid connection, the placement of the new resonant frequency needs careful consideration as it may be significantly higher, influenced by a smaller capacitance (C_p). For a 10:1 C_s/C_p ratio, the new resonant frequency may three times higher than for the passive LCL.

The problem can be explained by considering the harmonic current spectrum produced by the VSI that needs to be removed. The triangular shape of the current ripple means that the first harmonic will cause the largest sidebands around the switching frequency and the remaining harmonic clusters situated around multiples of the switching frequency with negligible amplitudes above 5kHz.

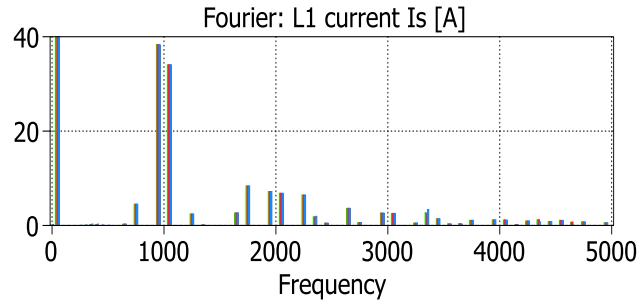

Fig. 8. VSI (L1) inductor current harmonics

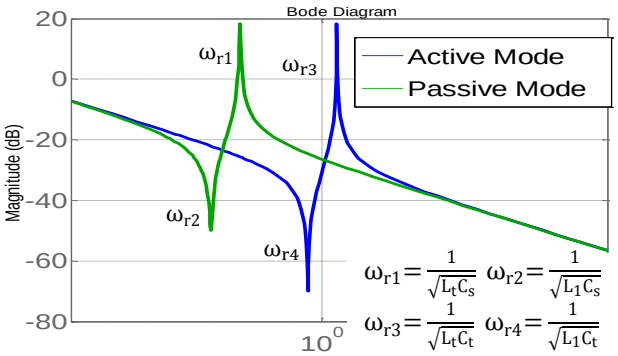

Fig. 9. Converter Voltage to Converter Current Bode plot for active and passive filtering mode. (the frequency scale is logarithmic in [kHz])

In a stiff grid situation, the CSI design is implemented by matching the parallel capacitance Cp as a fraction of Cs to limit the circulating current and then choosing an appropriate filter inductance to place the cut-off frequency at less than half of the CSI switching frequency (typically 10-15 kHz for 30 kHz CSI switching frequency). This means that the CSI filter produces no/constant attenuation for the VSI current ripple (f<5 kHz) to be cancelled (Fig.8).

In the LCL scenario, the connection of capacitance C_p to C_s will mitigate the resonant frequency of the LCL filter. Fig. 9 illustrates the resonant frequency mitigation by showing the Bode plot of converter voltage V_s to current I_s with the corresponding resonances for active and passive mode.

Considering that the resonant frequency of a medium voltage LCL filter is typically situated around half of the most significant lowest switching frequency harmonic, it makes it impossible to place the new resonant frequency ω_{r3} outside of the current harmonic range to be cancelled shown in Fig. 9. Placing the resonance below the switching frequency sidebands is impossible as it would require a much larger capacitance ratio compared to C_s and placing the resonance above 5 kHz is also not feasible as the capacitance would be too small causing large switching harmonic voltage across it.

The capacitance value must therefore be selected to avoid placing the resonant frequency where a switching current harmonic is situated as this could excite resonance and would create instability. In this case the suggested value would be near 1.5 kHz, equally spaced between the harmonic clusters of the switching frequency and twice switching frequency. For the following design however C_p has been chosen at 10µF placing the resonant frequency at 1190Hz, close to the 1250Hz sideband in order to demonstrate that stable circuit operation is possible under certain damping options which means the component design is not so strict.

C. Passive damping

One option of dealing with resonance is via the use of passive damping. Fig. 10 reveals three possible damping options and Fig. 11 shows the corresponding frequency response on the input voltage to input current for the values listed below.

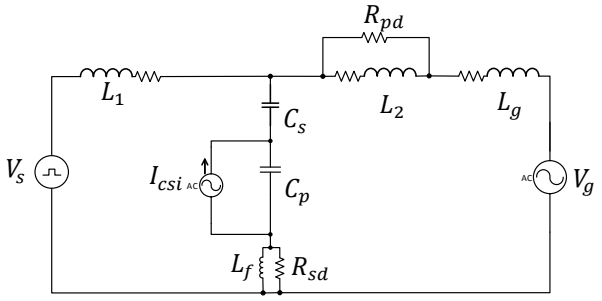

Fig. 10. Single Phase Equivalent circuit showing passive damping options

- L_2 parallel damping resistor R_{pd} =50Ω
- Series capacitor damping resistor R_{sd} =1Ω
- Series capacitor LR damping R_{sd} =1Ω, L_f =0.3mH

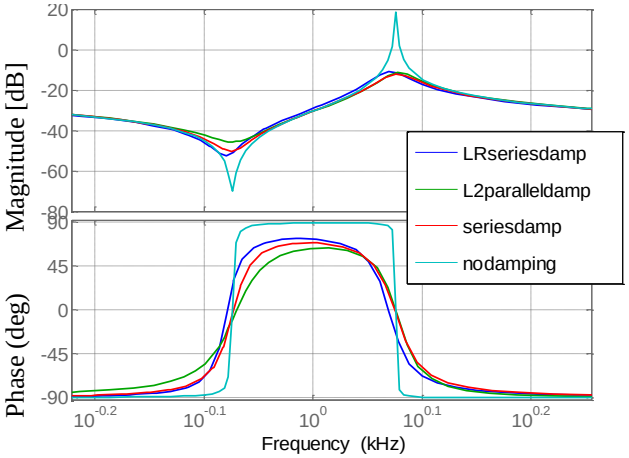

Fig. 11. Frequency response under different passive damping scenarios

The option of adding a parallel resistance to L_2 is effective, but as the parallel resistor cannot be removed during passive mode the losses are increased. Thus one of the other two methods could be pursued with the advantage that if critical damping can be achieved, the CSI control circuit remains the same as in the stiff grid situation. Realistically, some damping is achieved by the internal AC resistance of the components, which for high current rating inductors (L_1, L_2, L_g) may have significant skin effect around 1kHz. But the addition of extra damping resistance would lead to additional cost and losses, making passive damping undesired.

D. Active damping

The high switching frequency and application of the CSI in this hybrid topology to cancel the switching disturbance means that any resonance which is situated within the bandwidth of the controller should theoretically be contained by default. The placement of the resonant frequency within the current spectrum of harmonics to be eliminated means that using only the gain stated in (4) is no longer sufficient and that the frequency characteristic of the CSI to grid current needs to be considered in order to achieve stability.

This task however is not straightforward due to the associated phase characteristic at around the resonant frequency. Unlike active damping requirements in other applications which are focused mainly on the reduction of the gain characteristic at the resonant frequency, this application requires that the phase characteristic of the converter side current must be maintained and reproduced accurately in order for the ripple cancellation to take place. As a result a closed loop control system approach must be put in place to achieve unity gain and zero phase characteristic throughout the frequency range of interest.

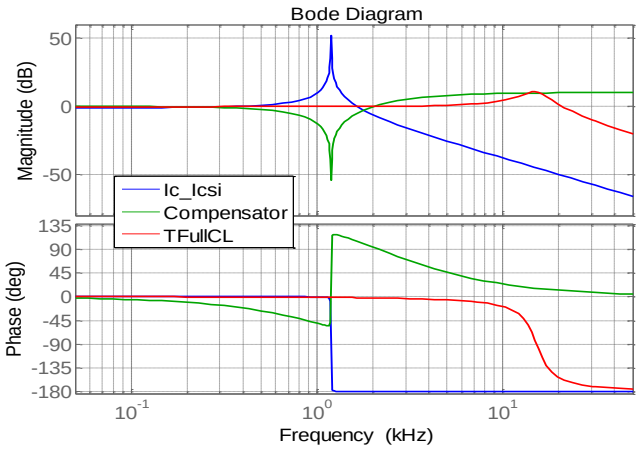

Fig. 12. Bode plots of the following transfer functions: Icsi to Ic, the resonance compensator and the overall closed loop active damped system

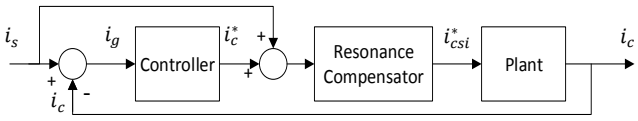

Fig. 13. Active damping implementation for Ripple Cancellation

Fig. 12 shows the proposed active damping control system while Fig 13 shows separately, the corresponding Bode plots of the Plant (I_c/I_{csi}), of the resonance compensator and of the overall closed loop response. The switching current ripple extracted from the main converter (L_1) current i_s is the reference signal for the series capacitor current i_c. The resonance compensator acts as a notch filter at the resonant frequency as shown in Fig 13. The controller is designed so that the closed loop response behaves like a low pass filter with cut-off frequency around 15kHz and zero or negligible phase shift up to 5 kHz. The actual implementation means that the "Eq (4)" block in Fig. 4 is replaced with the resonance compensator.

V.SIMULATION RESULTS

The performance evaluation of the proposed hybrid system shown in Fig. 2 is carried out by implementing the simulation model and the control in Plecs. The first step includes a test to validate the operation of the active damping control system shown above. Steady state harmonic performance is evaluated in terms of grid current and PCC voltage quality. A solution is explored to remove the PCC voltage ripple caused by CSI switching including also the assessment of grid impedance variation. Finally the semiconductor losses are estimated to estimate the full impact of adding the auxiliary CSI to the system.

A. Validation of the Active damping compensator

Fig. 14 reveals the transient performance of the system when operation is changed from passive LCL filtering mode (t<0.28s) to activation of the CSI (t1=0.28s) followed by a rapid build-up of resonance of the LC circuit that include the small CSI filter capacitor Cf and result in a resonant frequency in the proximity of the upper switching sideband which makes things worse but was deliberately chosen to demonstrate the effectiveness of the active damping compensator which is activated at t2=0.36 and facilitates full damping of the resonance (t>0.7s) without involving any dissipative element (damping resistance).

In order to assess accurately the performance, the grid currents were sampled at key moments during this transient and the resulting grid current FFTs are shown in Fig. 14b-d. All three FFTs are performed on a 20ms window (one grid frequency period). In figures 14b and 14d, the system is operating in steady (passive LCL filtering in Fig. 14b) or near steady state conditions (hybrid filtering Fig. 14.d) therefore the FFT is indicative of the attenuation of the harmonic filter (passive or active). In Fig 14c, the FFT has been performed on a 20ms window during the peak of the transient to show the rapid build-up of resonance and hence the larger current scale. It can be observed th at passive LCL filtering mode offers a good power quality with the highest switching harmonic being reduced from 38Apk (Fig. 8) to 3.2Apk which means by almost 12 times (-21.5dB). A residual current harmonic is present at approx. 750Hz that corresponds to the resonance frequency of the LC circuit formed by the grid/main inverter

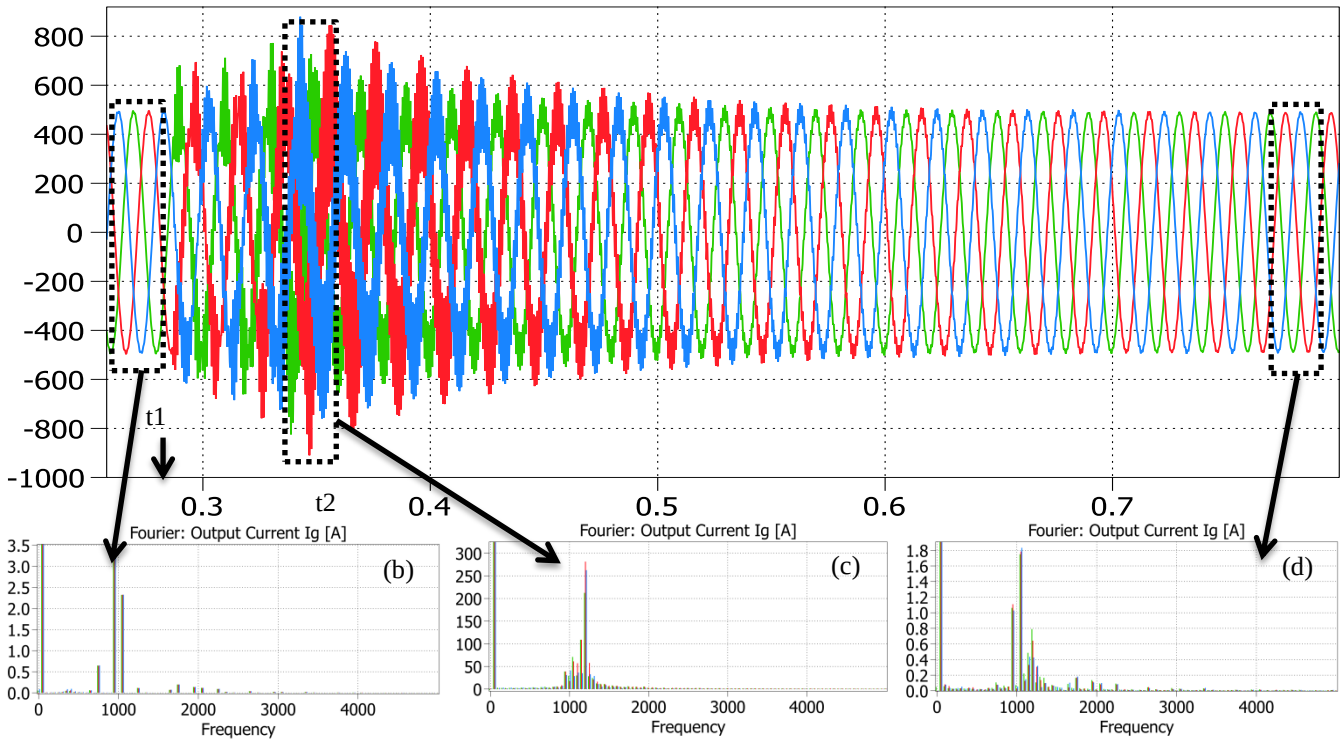

Fig. 14. Transient operation showing activation of CSI at t1=0.28s followed by LC circuit resonance build-up and activation of the resonance compensator at t2=0.36s followed by resonance being actively damped (t>0.7s). b)-c)-d) FFT of the MV grid currents when b) CSI was off and switching ripple is passively damped by the LCL filter; c) just before active damping activation (t=0.34-0.36); d) at end of simulation when resonance levels are not visible.

inductance and the series capacitor Cs. The X/R ratio considered however provides sufficient damping to this circuit and the resonant harmonic stays reasonably low.

When active filtering is enabled and after the resonance damped, it can be noticed that same switching harmonic considered before (950Hz) is reduced to $1.1A_{pk}$ which by a factor of 34.5 (-30.8dB). However, the most important harmonic is the upper sideband which peaks at 1.8A which corresponds to a smaller attenuation compared to Fig. 8 and the cause is that the active damping compensator of the LC filter having a resonance at 1.25kHz, very close to the upper side that needs to be attenuated, is altering the active filter behaviour of the circuit. This can be improved by decreasing the CSI filter capacitor so that the resultant resonant frequency is moved at 1.5 kHz, equally spaced between upper switching frequency sideband and lower twice the switching frequency sideband. This would minimise the interaction between the resonant compensator and the active filter at the relevant switching harmonics.

B. Transient and steady state results

The choice of placement of the resonant frequency in the previous test has been done to demonstrate the functionality of the resonant compensator in a worst case scenario but this does not result in the best filtering performance of the hybrid system in steady state conditions. To achieve best performance, the system has been retuned in order to place the resonant frequency at a optimal point which is the equally spaced from the largest current harmonics of main VSI. Capacitor Cs remains unchanged at 100µF while the redesign of the filter required a Cp of 7µF to move the resonant frequency from 375Hz during LCL passive mode to 1.46 kHz during active filtering mode.

A similar procedure to enable the operation of the auxiliary CSI has been repeated with the resonance compensator activated immediately when transitioning from passive to active filtering. To make the implementation as realistic as possible, the following changes in the simulation models have been implemented for the following tests: a deadtime of 1µs has been used for the main VSI; an overlap time of 300ns has been used for the CSI; a 20mH inductor was connected to the CSI DC-link and an overvoltage protection clamp circuit set at 1kV for protection of the CSI switches was also added. The reason why the distortion of main VSI current due to deadtime is not so obvious is that its influence is much smaller at low switching frequencies and this also decreases with the increase of number of levels.

Fig 15 a-d reveals the transition from passive filtering to active filtering at time t1 (@0.5s) by showing the series capacitor and CSI voltages as well as series capacitor currents. During the transition, a surge of currents in the clamp circuit is noticed as well as an overshoot of the CSI DC-link current but the CSI peak voltages is limited to 1kV. It can be observed that once active filtering is activated, the fundamental voltage component that is proportional with the fundamental current passing through capacitor Cs will be slightly reduced with the difference being shared with the CSI.

Fig 16a-b shows the details at the end of the simulation in Fig. 15, when the models reached steady state. The voltages seen on the AC side of the CSI when the hybrid converter operates in active filtering mode are below 1kV, in line with the design

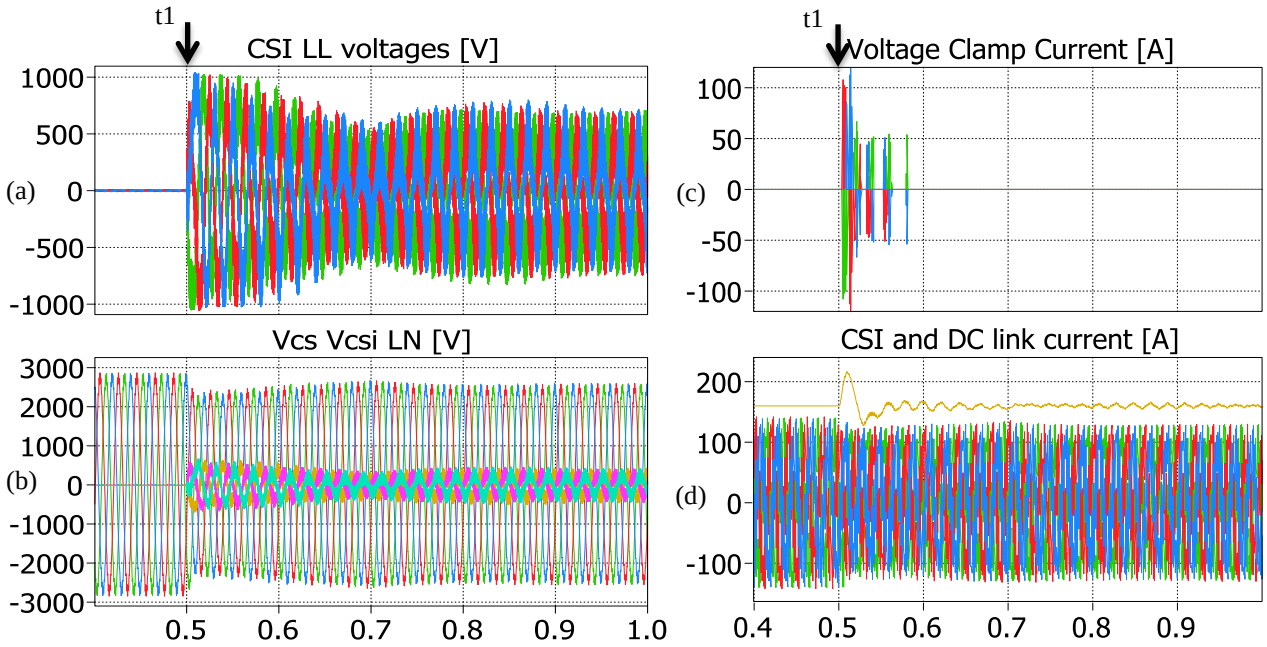

Fig. 15a-d. Transient between passive and active filtering mode at t1 showing a)CSI l-l voltage b)Series capacitor and CSI phase voltages c)Voltage clamp current and d) Series capacitor current along with CSI DC link current.

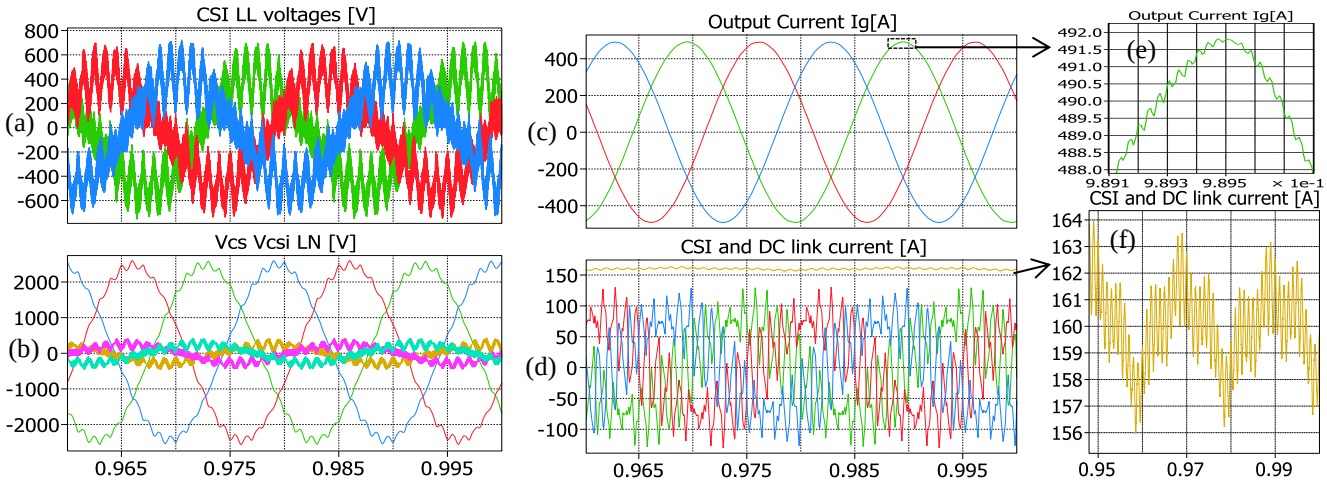

Fig. 16a-f. Zoom in on waveforms shown in fig 17 showing steady state conditions during active filtering mode showing a)CSI l-l voltage b)Series capacitor and CSI phase voltages c)Output current d) Series capacitor current e)zoom in on output current and f) further zoom in DC link current

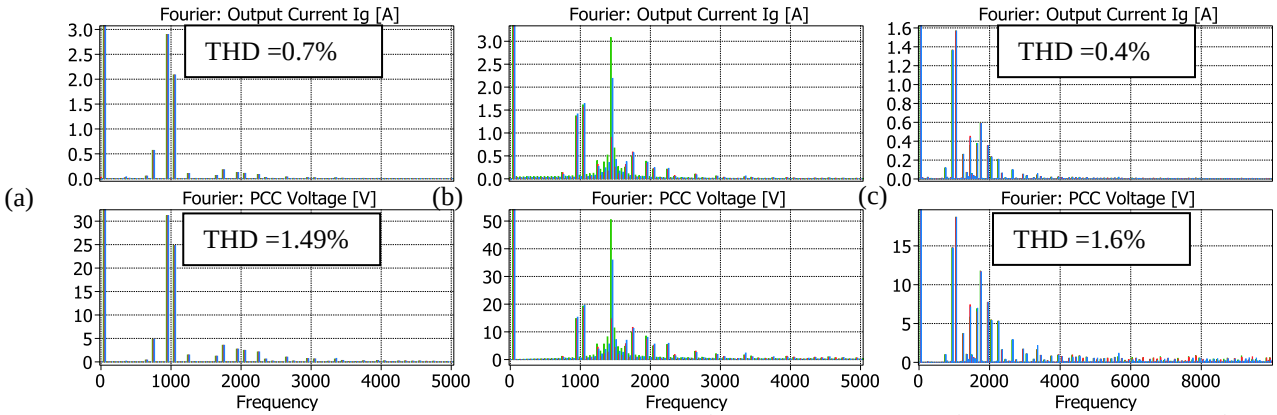

Fig. 17 a-c. Output current and PCC voltage harmonic content (corresponding to fig 15b-d) a)during passive filtering mode b)during active filtering transient showing resonance excitation and finally c) showing steady state performance during active filtering.

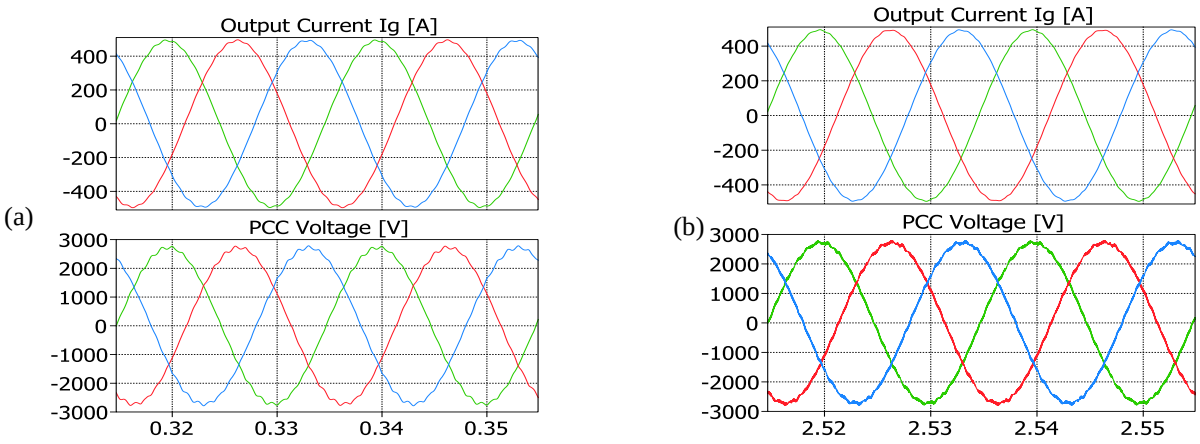

Fig. 18a-b. Steady state output current and PCC voltage a)during passive filtering mode and b)during active filtering

specification with the fundamental component remaining at 10% of the voltage at the point of connection. Fig 16c reveals that the main inverter switching ripple is significantly improved while in Fig 16e which is a zoom in shows that there is still some residual ripple remaining but this is at the CSI switching frequency of 30 kHz. Fig16d reveals the CSI current through the series capacitor along with the DC-link current during steady state. A closer look on the DC link current shown in Fig 16f shows that its average remains at the 160A reference value having harmonics at the switching frequency and twice the fundamental frequency (100Hz). The overall peak to peak ripple is approximately 5% of the DC reference value.

The harmonic content for significant frequency components less than 10 kHz is shown in Fig 17 on the output grid current and voltage at the point of common coupling (PCC) at different moments during the transient performed in Fig 15. Fig 17a reveals the harmonic content during passive filtering which results in a current THD of 0.7% and voltage THD of 1.49%. Once active filtering is enabled, an expected small resonance excitation can be observed in both the output current and voltage as shown in Fig 17b. Finally Fig 17c reveals the harmonic content close to steady state (t=1s) with the highest current harmonic reduced to 1.6A and a resulting grid current THD of 0.4%. Although the voltage harmonic content appears to be reduced around 1kHz, the THD appears to be slightly increased at 1.6% compared to 1.49% during passive filtering.

This can be seen more clearly in Fig 18a-b showing steady state waveforms during passive and active filtering. In passive mode (Fig 18a) a small ripple can be observed in both current and voltage waveforms. During active filtering the ripple caused by the 1 kHz VSI switching will be mitigated by the CSI at the cost of injecting a small 30 kHz current ripple. On the output current this is barely noticeable due to the high impedance of the filters. However, due to the same large grid impedance, this small 30 kHz residual CSI current ripple that escapes into the AC grid causes a noticeable voltage ripple at PCC which requires additional consideration.

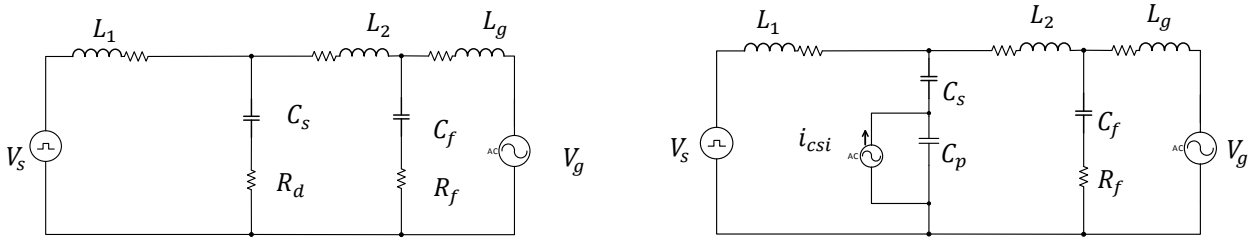

Fig. 19. Single Phase Equivalent Circuit with output RC filter during passive filtering (left) and during active filtering (right)

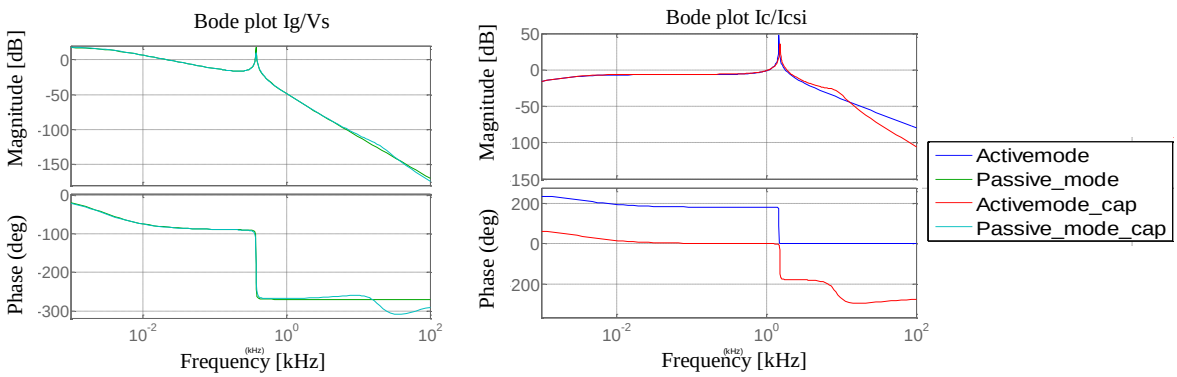

Fig. 20. Bode plot showing Gain Vs frequency for Ig/Vs (VSI behaviour) as well as Ig/Icsi(CSI behaviour) with and without RC filter.

C. PCC voltage ripple removal and assessing the effect of Grid impedance variation

To assess the possibility of addressing this PCC voltage ripple issue, an investigation is presented regarding the possible introduction of a shunt capacitance at the point of common coupling to prevent the 30 kHz switching harmonics from being injected in the grid as shown in the single phase equivalent circuits in Fig 19.

The requirement for this capacitance is to be smaller than Capacitor Cp so that the additional resonance is generated at a higher frequency well above the main resonance of 1.46 kHz (5-10kHz). The 30 kHz voltage harmonic amplitude is small and high enough in frequency so that a small capacitance in combination with a damping resistor to prevent resonances can provide sufficient attenuation while meeting the requirement of no interference with the fundamental voltage component. To demonstrate this, two situations are compared: with a 1μF capacitance Cf along with a resistance Rf of 10Ω and without. The resulting frequency responses are plotted in Fig 20 for VSI voltage to grid current and CSI current to output current. Although the equivalent circuit for passive filtering shown in Fig 19 suggests a fifth order response, the capacitance is small enough to have a negligible effect on the output harmonics produced. The addition of the RC circuit becomes apparent on the CSI transfer function where the additional resonance can be observed as well as a slight shift in the main resonant frequency.

D. Grid inductance Variation

The relatively low SCR chosen resulting in an output inductance ratio of 1 (L2: Lg) means that the addition of any capacitive element at the PCC will have a significant effect on the main resonant frequency reducing the effectiveness of the active damping compensator. This is also true of any fluctuations in grid inductance indicating that the proposed system is not ideally suited for weak grid situations where the grid inductance is significantly large compared to the line side inductance. This is not the case for a higher inductance ratio where the shift in resonance is less significant although it would still result in a small error around the resonant frequency. In order to demonstrate the effect of grid variations on the active damping compensator the circuit has been simulated using the above Cf/Rf combination starting with an inductance ratio of 3:5 (L2=2.8mH and Lg=0.8mH). Subsequently a 50% decrease in the grid inductance to Lg=0.4mH has also been simulated to verify that for the given situation, there is reasonable tolerance to grid impedance variations. Figure 21a shows the output PCC voltages as well as grid currents without capacitor Cf where the highest harmonic amplitude around 30kHz is around 12V as shown in Fig. 22a. Figures 21b-c and their FFT in Fig. 22 b-c show the effectiveness of Capacitor Cf in attenuating the 30 kHz voltage to negligible levels with some improvement evident also around the 1kHz frequency harmonics.

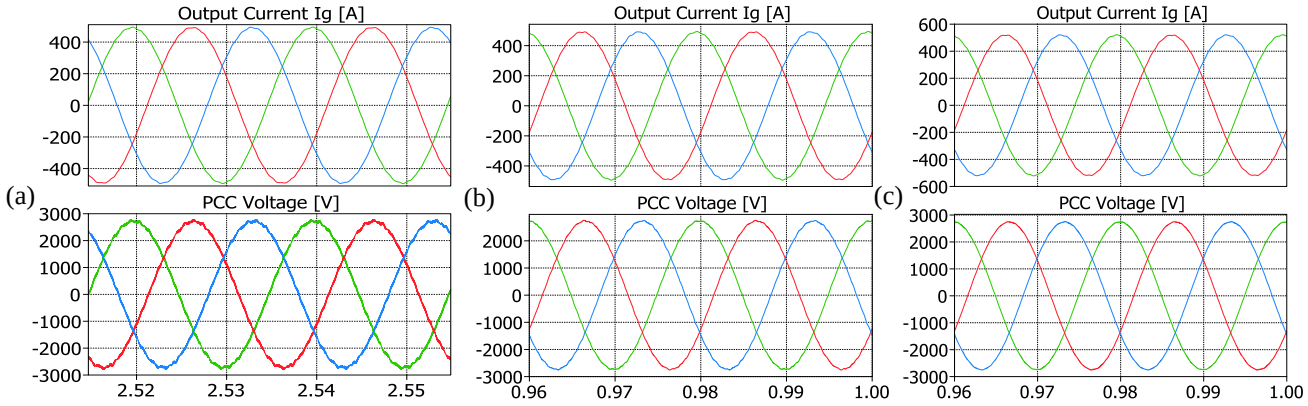

Fig. 21a-c. Steady state output current and PCC voltage during active filtering a)without voltage filtering b)Using Cf/Rf and L2=2.8mH, Lg=0.8mH and using Cf/Rf and L2=2.8mH, Lg=0.4mH (50% grid impedance variation)

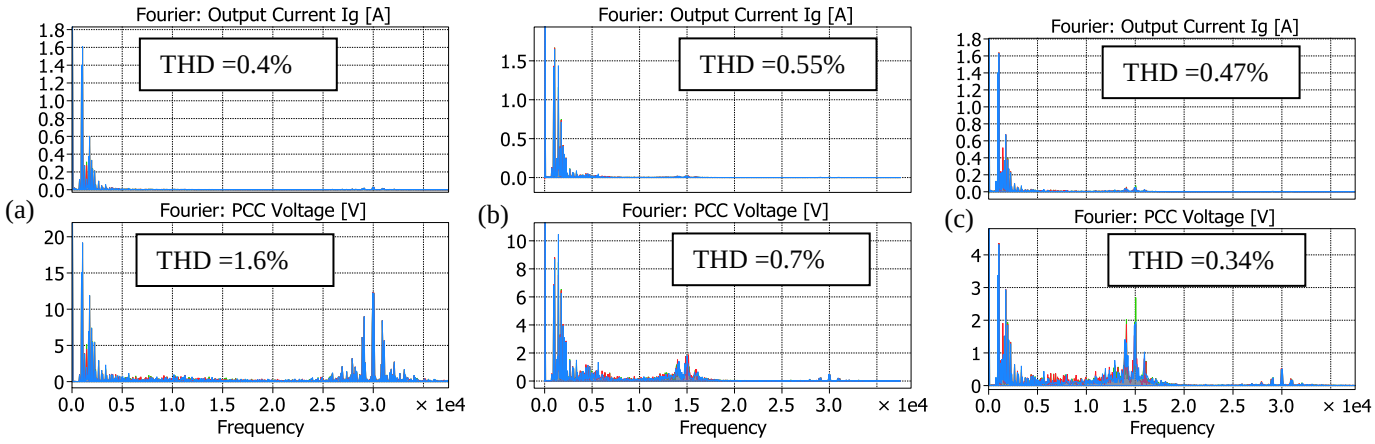

Fig. 22a-c. Output current and PCC voltage harmonic content during active filtering a)without voltage filtering b)Using Cf/Rf and L2=2.8mH, Lg=0.8mH and using Cf/Rf and L2=2.8mH, Lg=0.4mH (50% grid impedance variation)

As the presence of the additional output capacitance has not been accounted for in the active damping compensator, it therefore creates an error around the 1.4 kHz resonant frequency in conjunction with the grid impedance variation.

This is indicated by the slight increase in the output grid current THD. When the output impedance is reduced further from 0.8 to 0.4mH, the compensator error seems to be reduced around 1 kHz as the resonant frequency moves towards lower frequencies although with a slight harmonic increase at 15 kHz due to a resonance created by the controller. It can be concluded that the addition of Cf is highly effective providing high PCC voltage quality along with high current quality with some flexibility towards grid impedance variations given that the ratio of line inductance is higher than the grid inductance.

E. Semiconductor Loss estimation

To evaluate the increase of system losses, the semiconductor power loss models have been used to estimate semiconductor losses. First, a realistic pair of power switches has been chosen: the VSI FF400R33KF2C IGBTs from Infineon have been chosen, rated at 3.3kV/400A while for the CSI, the Semikron SEMiX202GB12E4s 1.2kV/200A have been chosen. With this choice, the added installed power in the CSI active switches as calculated in [11] reaches 4.5%.

The total semiconductor losses during steady state operation are summarised in Table 3. Both VSI and CSI have similar distribution of switching and conduction losses indicating good loading of the switches. The total losses amount to 1% of the system output power (approx 2MVA) with the VSI dissipating 14.3kW and the CSI 2.7kW which is 15.4% of the VSI losses, a level that can be considered as reasonable and typical also for the losses expected in passive filters.

For a standalone VSI system that would produce the same semiconductor losses, the equivalent switching frequency will be around 1.35 kHz which will result in a limited reduction of the current ripple, significantly inferior to what the hybrid approach offers. It can therefore be concluded that the use of the CSI is done at the lowest possible cost with respect to efficiency.

TABLE III: ESTIMATED SEMICONDUCTOR LOSSES IN KW

	Conduction	Switching	Total
VSI losses	7,201	7,131	14,332
CSI losses	1,330	1,284	2,615 (15.4%)
Total			16,947

F. Added Installed Power

Based on the steady state operating condition shown in Fig. 16 and the peak voltage and current stress values of 3.3kV/490A for the VSI and 700V/164A for the CSI, the added installed power is given by (6) at less than 3.6%, in line with the theoretical calculations indicating.

$$Added\ Installed\ Power\ [\%] = \frac{\#\ of\ CSI\ switches * CSI\ \widehat{voltage}\ stress * CSI\ \widehat{current}\ stress}{\#\ of\ VSI\ switches * VSI\ \widehat{voltage}\ stress * VSI\ \widehat{current}\ stress} * 100 \qquad (6)$$

The series capacitor is rated at 12% of the VSI output power, mainly contributed by the 50Hz component, at less than the 20% limit imposed in the design, which in terms of stress is similar to a capacitor in a standalone LCL installation. Although some additional cost will be added towards the CSI voltage protection circuit the overall installation cost is at a minimum for a medium voltage system.

VI. Experimental Results

To verify the validity of the hybrid converter system in its ability to cancel the switching ripple currents of the main converter by using a low voltage/low current rated CSI, a laboratory prototype was built. The diagram of the laboratory setup currently in development is shown in Fig. 23 with component values as well as system settings shown in table IV The preliminary experimental validation has been done at 70% grid voltage (290Vrms line-to-line voltage resulting in approx. 240V peak voltage. The dc-link voltage of the VSI was 450V and the input power processed was approx. 3kW.

Figure 24a-b shows the start-up behaviour of the hybrid system with the CSI initially disabled and after start-up, set to control only the series capacitor voltage drop (no switching harmonic injection) with voltage drop coefficient K=10%. It should be noted that the evaluation was in fact done with the VSI operating with a much higher value for the relative current ripple (37%) compared to the simulation (20%) which artificially increases the installed CSI power but the aim for these tests was to have the opportunity to cancel a large switching ripple that would make the cancelation obvious as it is the case.

Fig 24b shows the phase to neutral supply voltage, the series capacitor voltage and the CSI phase voltage. Prior to start-up (t0), the series capacitor voltage is small, with all supply voltage being seen across the CSI inputs. In a real implementation, the CSI will be fully shorted before start-up to prevent higher voltages being seen at the CSI inputs and allow the use of devices rated below grid voltage. After activation, the series capacitor voltage raises to 220Vpkwhilst the CSI phase voltage falls to 26Vrms with highest recorded peak at 56V amounting to 23% of the grid.

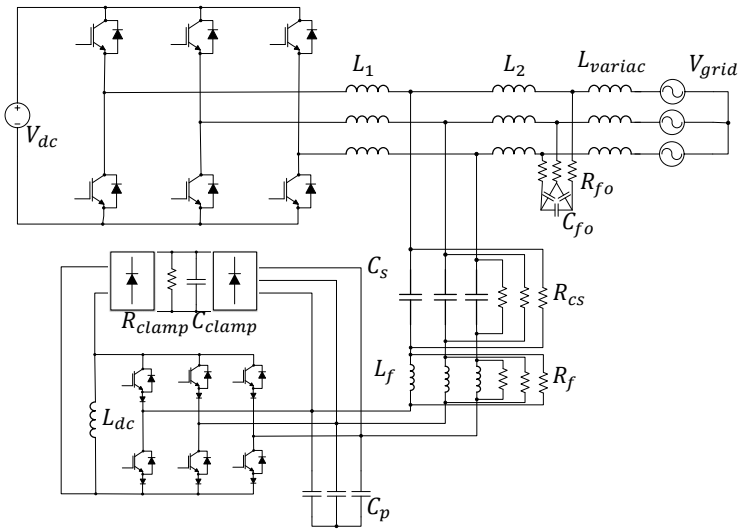

Fig. 23. Experimental Setup circuit diagram

TABLE V: COMPONENT VALUES AND SYSTEM SETTINGS FOR EXPERIMENTAL VALIDATION

C_s	C_p	C_{clamp}	V_{dc}	V_{grid}
12µF	1µF	20µH	450V	290V
L_1	L_2	L_f	L_{dc}	L_{variac}
11mH	280µH	300µH	30mH	~0.6mH
R_f	R_{cs}	R_{clamp}	R_{fo}	C_{fo}
50Ω	100kΩ	100kΩ	33Ω	180nF
Ivsi	Idc	K	f_{sw}^{VSI}	f_{sw}^{CSI}
8Apk	4.5A	10%	1 kHz	25 kHz

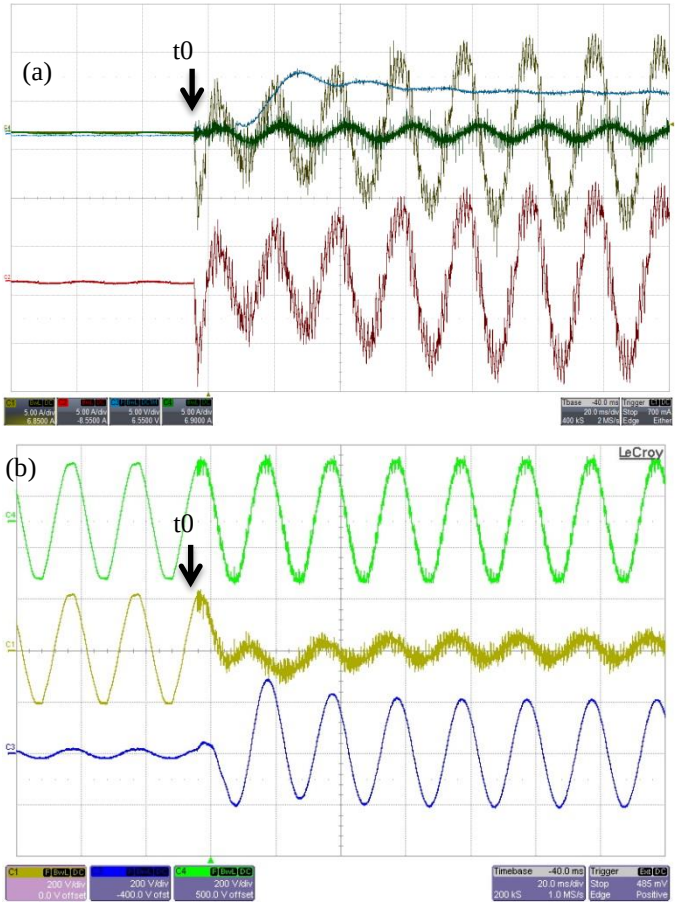

Fig. 24a-b. Experimental results showing transient performance during turn on for Phase A a)VSI current (yellow), CSI output current(green), CSI DC-link current(blue) and combined grid current(red) with b) corresponding Grid voltage(green), CSI voltage(yellow) and series capacitor voltage(blue)

Time scale: 20ms/div Currents 5A/div Voltages 200V/div

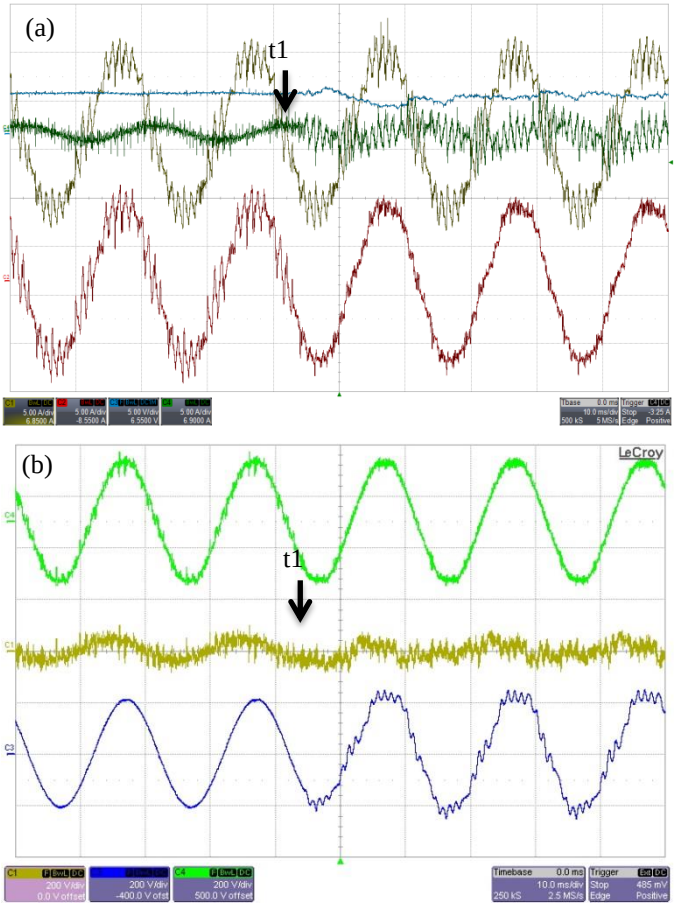

Fig. 25a-b. Experimental results showing transient performance during starting of harmonic cancellation for Phase A a)VSI current (yellow), CSI output current(green), CSI DC-link current(blue) and combined grid current(red) with b) corresponding Grid voltage(green), CSI voltage(yellow) and series capacitor voltage(blue)

Time scale: 10ms/div Currents 5A/div Voltages 200V/div

Fig. 24a shows the CSI dc -link current, the CSI current in phase A, the VSI current in phase A and the cumulated grid current. The fundamental component of the VSI current is approximately 8Apk consistent with a 5.6Arms fundamental which results in a power processed of 2.85kW. The CSI current is mainly fundamental (< 1Apk) and its own switching ripple. The grid current shows similar harmonics as the VSI currents since the CSI current is much smaller and harmonic cancelation is not active.

The activation of the harmonic cancelation is shown in Fig. 25a-b. Fig 25b shows the supply voltage, the CSI voltage across phase A input filter capacitor and the voltage across the phase A series capacitor. Activation of the active filtering takes place at t1. Before activation, both the CSI voltage and the series capacitor voltage are mainly sinusoidal, with some low order 5^{th} and 7^{th} harmonics resulting in flat tops due to the grid whilst the supply voltage seen across the autotransformer shows a noticeable content of 1 kHz harmonics caused by the VSI switching ripple.

After activation, the CSI voltage is significantly distorted. The voltage harmonics are caused by the CSI current injected though the series capacitors, which are also visible in the series voltage capacitors. The supply voltage seen at the outputs of the autotransformer is noticeably cleaner, which is a clear sign that most VSI switching current ripple has been successfully cancelled by the CSI. The effectiveness of the current cancelation is fully disclosed by the current waveforms shown in Fig 25a. The cumulated grid current shows no VSI switching ripple. The improvement in quality is much clearer when the FFT of the VSI current and the cumulated grid current are compared (Fig26), with a 4-5 times reduction (900Hz harmonic is reduced from 5.5 to 1 div, 1100Hz harmonic is reduced from 5 to 1.2 div).

In terms of CSI ratings, it can be noted that during the active filtering, the CSI phase voltage exhibits a peak of 74V which is 30% of the peak grid voltage whilst the ratio becomes 15.5% if the ratio is evaluated by using the RMS voltages (the oscilloscope indicated 26V compared to the corresponding supply phase voltage of 166Vrms). The FFT of the CSI voltage shown in Fig 27 shows the fundamental harmonic amplitude at 20V at 8% of the grid voltage within the 10% voltage coefficient chosen. The peak current processed by the CSI is the DC-link current (5A) which is 0.44 of the 11.25A peak of the VSI currents. The ratio of RMS currents is 0.22 (1.34Arms (CSI) / 5.86Arms (VSI).

To investigate the impact of adding the auxiliary system on losses and power factor the system has been benchmarked using a power analyser with the VSI operating standalone whilst measuring input/output power. The standalone VSI efficiency was recorded at 94.31% at a PF=1 compared to efficiency of 93.24% and PF of 99.3% with the added CSI system in full operation. The added losses of the CSI (~32W) are at 1.1% of the input power indicating that the CSI improvement in harmonic performance comes at a minimum power loss and minimal impact on the output power factor therefore validating the system.

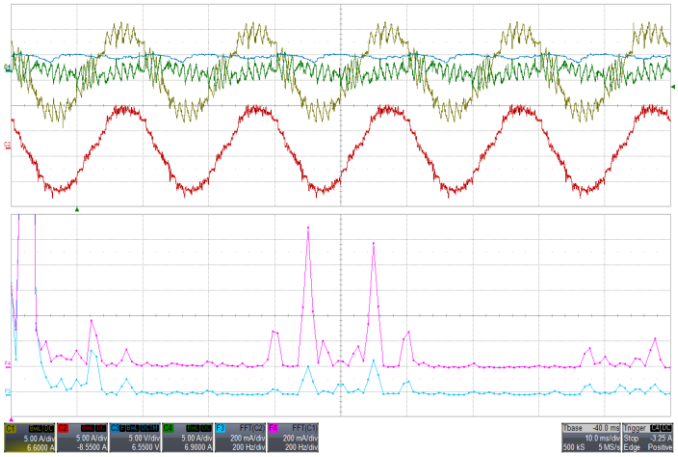

Fig. 26. Experimental results showing steady state performance

Top: VSI current (yellow), CSI output current(green), CSI DC-link current(blue) and combined grid current(red) for 5 cycles (Top) Time scale: 10ms/div Current Amplitude: 5A/div

Bottom: Corresponding FFT of VSI current(pink) and combined grid current(blue) Frequency scale: 200Hz/div Amplitude: 200mA/div

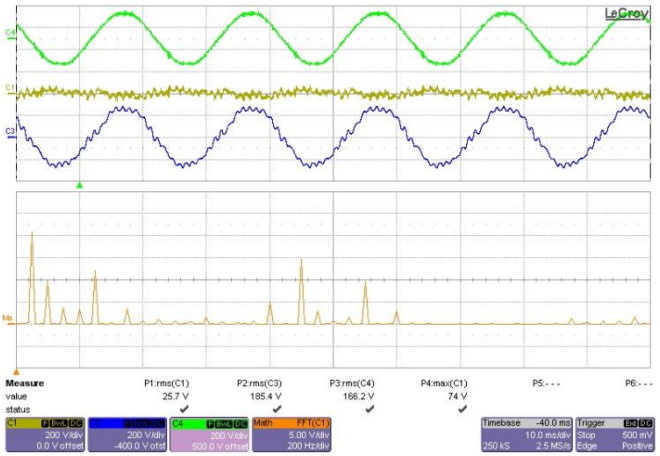

Fig. 27. Experimental results showing steady state performance

Top: Grid voltage(green), CSI voltage(yellow) and series capacitor voltage(blue) for 5 cycles (Top) Time scale:10ms/div Voltage Amplitude 200V/div

Bottom: Corresponding FFT of CSI voltage(orange) Frequency scale: 200Hz/div Amplitude: 5V/div

VII. CONCLUSIONS

This paper validates the feasibility of the hybrid concept resulting by adding an auxiliary CSI to a medium voltage LCL filter to enhance the switching ripple cancellation while maintaining low installed power on the CSI. The design criteria to achieve low installed power in the CSI that are defining the design of the hybrid system with a stiff grid have been introduced and validated by simulations.

The LCL-CSI connection scenario which is relevant for upgrading existing MV inverter installations introduces some new design challenges related to LC resonance, which have been explored in this paper. To address this challenge, a resonance compensator that behaves similar to a notch filter on the resonance but guarantees zero phase-shift in the frequency range of interest for the switching ripple has been added to the control structure.

To validate the effectiveness of the proposed resonance compensator, the resonant frequency of the hybrid system has been intentionally placed near the biggest VSI current harmonics in order to demonstrate that the design requirements are not strict as long as the compensator is properly designed but the attenuation performance of the switching ripple nearest to the resonant frequency is affected. This is proven via a set of transient simulation tests by enabling the resonance compensator after the CSI was enabled and a resonance has build-up, followed by an effective removal of the resonance after the compensator was activated. Proper placement of the resonant frequencies allows for even better filtering performance. Further investigations into improving the voltage quality affected by the residual CSI switching current ripple in conjunction with high impedances due to high switching CSI frequencies have also been investigated. A study of the semiconductor power losses revealed a reasonable increase of 15% which is justified by the improved attenuation of the hybrid active filter while the added installed power remains under 4%.

Finally preliminary experimental validation of the system has been provided at 3kW with the CSI performance showing a fivefold reduction in switching harmonics at the VSI switching frequency while operating at 30% of the grid voltage. Added system losses amount to 1.1% showing minimal impact on the overall output power for the power quality improvement offered.

VIII. REFERENCES

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